In the Specification

Please amend the following specified paragraphs as indicated below.

Page 1, after the title, please insert the following:

This is a division of US App. No.10/085,689 filed February 27, 2002 and issued September 9, 2003 as US Pat. No. 6,617,222.

[0022] Various embodiments of the invention provide a hemispherical silicon grain (HSG) polysilicon inhibitor layer over selected locations of the smooth polysilicon to inhibit HSG growth in those locations during HSG conversions of other locations of the smooth polysilicon. The processes described herein may reduce the likelihood of HSG polysilicon flaking from the container capacitor bottom plate, ~~and~~ thereby reducing defects resulting ~~therefrom~~ from this flaking. Various inventive processes described herein may also reduce the likelihood of bridging of the HSG polysilicon between adjacent container capacitor storage plates.

[0024] In one embodiment of the invention, the smooth polysilicon layer is formed in a continuous layer but is more heavily doped, for example with phosphorous, as it is initially formed. As the thickness increases during its formation, less dopant is integrated into the layer. This ensures an adequate electrical connection between pad ~~32~~ 28 and the bottom plate 40. The portion of the layer formed first, which has the heaviest doping, may be doped to between about 1 E^{18} atoms/cm^3 to about 1 E^{21} atoms/cm^3. The portion of the layer formed last will, typically, remain undoped ~~not typically doped~~ or may be only minimally doped. The layer is formed as a continuously thick layer, but comprises a decreasing gradient of doping from the bottom to the top of the layer. Having little or no doping at the top of the smooth polysilicon layer provides a resulting HSG layer which is of higher quality than an HSG layer which is formed from a doped smooth polysilicon layer. A conductive layer of conductively-doped polycrystalline silicon 40 between about 50Å and about 150Å may be formed using plasma enhance chemical vapor deposition (PECVD) techniques. For example, silane gas (SiH_4) is introduced as a silicon source into a deposition chamber

at a flow rate of between about 400 sccm and about 600 sccm along with phosphine (PH_3) at a flow rate of between about 5 sccm and about 15 sccm at a temperature of between about 500°C and about 600°C for a duration of between about 2.5 minutes and about 15 minutes. Using this process the preferred material is formed at a rate of between about 10Å/min to about 20Å/min. As the layer forms the PH_3 flow rate may be decreased to 0 sccm over a period of about 10 seconds as the layer approaches about half its final thickness. This forms a layer 40 as depicted in FIG. 11 of between about 50Å and about 150Å thick.

[0029] While it is preferable that these materials form only at the locations depicted by structures 110 in FIG. 14, they may also form undesirably on the horizontal portions of the inside of the recess defined by the polysilicon layer as depicted by structures 112 in FIGS. 14-16. This layer 110, 112 will inhibit conversion of the polysilicon to HSG polysilicon at these locations, but the decrease in capacitance between the bottom and top plates of the completed capacitor will be minimal, as a majority of the bottom plate remains free from the inhibitor layer.